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Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (currently amended) A programmable processor comprising:

a data path capable of transmitting data;

an external interface operable to receive data from an external source and communicate the received data over the data path;

a register file containing a plurality of registers each having a register width, the register file coupled to the data path and operable to support processing of a plurality of threads and to store a plurality of data elements in partitioned fields, each of the data elements having an elemental width smaller than the register width;

an execution unit coupled to the data path, the execution unit operable to execute a plurality of instruction streams from the plurality of threads, each instruction stream including a single instruction that specifies an operation to cause multiple instances of the operation to be performed, each instance of the operation to be performed using a different one of ~~, the operation to be performed on each one of a~~ the plurality of data elements in partitioned fields of at least one of the registers to produce a catenated result~~, each of the data elements having an elemental width smaller than the register width~~.

2. (original) The processor of claim 1 wherein the execution unit comprises a pipeline having a plurality of stages and wherein the pipeline interleaves execution of instructions from the plurality of instruction streams.

3. (original) The processor of claim 2 wherein the pipeline is operable to simultaneously contain states of execution of at least two instructions from different instruction streams.